WHAT IS CLAIMED IS:

1. A data recovery apparatus, comprising:

a phase locked loop (PLL) for generating a plurality of phase clock signals each having a different delay time with respect to a clock signal;

an oversampler for M times oversampling serial input data in response to the plurality of phase clock signals and outputting a plurality of data bits in parallel;

a level transition detector for receiving the parallel data bits output from the oversampler, detecting the point of time at which the logic level transitions between adjacent ones of the parallel data bits and outputting the detection result as first through Mth transition signals;

a transition accumulator for accumulating the number of times each of the first through Mth transition signals is generated and outputting one of a first through Mth transition accumulation signal associated with the transition signal whose generation frequency is high;

a state selector for generating a state signal in response to the transition accumulation signal output from the transition accumulator, wherein the state signal is used for selecting data bits of corresponding positions among the parallel data bits output from the oversampler; and

a data selector for receiving the parallel data bits, utilizing the state signal to select from the parallel data bits those data bits having sampling positions corresponding to the state of the state signal, and outputting the selected data bits in parallel.

2. The data recovery apparatus of claim 1, wherein M is 3.

3. The data recovery apparatus of claim 2, wherein the level transition detector comprises:

a transition detector comprising a plurality of exclusive OR gates for performing an exclusive OR operation on two adjacent bits of the paralled data bits output from the oversampler and generating exclusive OR results as first, second, and third output signals; and

a transition detection signal outputting unit for processing the first, second, and third output signals to generate and output the processing results as the first through third transition signals.

4. The data recovery apparatus of claim 3, wherein the transition accumulator comprises:

a first accumulator for accumulating the first transition signal in response to the input clock signal and outputting a first transition accumulation signal at a first level when a predetermined number of first transition signals are accumulated;

a second accumulator for accumulating the second transition signal in response to the input clock signal and outputting a second transition accumulation signal at a first level when a predetermined number of second transition signals are accumulated;

a third accumulator for accumulating the third transition signal in response to the input clock signal and outputting a third transition accumulation signal at a first level when the accumulated number is a predetermined number; and

a reset signal generator for performing a logic combination on the first, second, and third transition accumulation signals and generating an accumulation reset signal for resetting the first, second, and third accumulators in response to the logic combination result.

5. The data recovery apparatus of claim 4, wherein the transition accumulator outputs one of the first, second, and third transition signal having the highest generation frequency as a corresponding one of the first, second, and third transition accumulation signals.

6. The data recovery apparatus of claim 4, wherein the state signal generated by the state selector comprises a first and second bit, wherein different combinations of the logic levels of the first and second bits are set based on which of the first, second and third transition accumulation signals is generated.

7. The data recovery apparatus of claim 6, wherein the first and second bits are respectively set to logic "0" and "1" when the first transition accumulation signal is generated, logic "1" and "0" when the second transition accumulation signal is generated, and logic "0" and "0" when the third transition accumulation signal is generated.

8. The data recovery apparatus of claim 7, wherein the data selector comprises a plurality of multiplexers, wherein each multiplexer receives M bits of the parallel data bits output from the oversampler and selectively outputs one bit among the M bits in response to the state signal.

9. The data recovery apparatus of claim 8, wherein when M bit data input to the plurality of multiplexers are represented to be 3P, 3P+1, and 3P+2, the data selector outputs the 3P+2th bits when the state signal is "01", outputs the 3Pth bits when the state signal is "10", and outputs the 3P+1th bits when the state signal is "00", wherein P is an integer not less than 0.

10. A data recovery method comprising the steps of:

(a) receiving as input serial data in blocks of K bits and performing an M times oversampling on each block of serial data using N phase clock signals having different delay times to output N data bits in parallel;

(b) detecting a transition in a level between adjacent ones of the N data bits and outputting one of a first through Mth transition signals at the point of time of a detected level transition;

(c) accumulating the number of generations of each of the first through Mth transition signals;

(d) detecting the transition signal whose generation frequency meets a predefined threshold; and

(e) selecting from the N data bits, K data bits corresponding to the detected transition signal.

11. The data recovery method of claim 10, wherein M is 3.

12. The data recovery method of claim 11, wherein K is 4 and N is 12.

13. The data recovery method of claim 11, further comprising the step of initializing the accumulating process upon detecting a transition signal.

14. The data recovery method of claim 11, wherein step (e) comprises the steps of:

selecting K oversampled data bits by one bit of a three-times oversampling position (3P+2) corresponding to the first transition signal when the first transition signal is detected in step (d);

selecting K oversampled data bits by one bit of an three times oversampling position (3P) corresponding to the second transition signal when the second transition signal is detected in step (d); and

selecting K oversampled data bits by one bit of a three times oversampling position (3P+1) corresponding to the third transition signal when third transition signal is detected in step (d).

15. The data recovery method of claim 10, wherein step (e) comprises the step of generating a state signal comprising a predetermined value based on the detected transition signal in step (d) and selecting the N data bits based on the value of the state signal.

16. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for recovering data, the method comprising the steps of:

(a) receiving as input serial data in blocks of K bits and performing an M times oversampling on each block of serial data using N phase clock signals having different delay times to output N data bits in parallel;

(b) detecting a transition in a level between adjacent ones of the N data bits and outputting one of a first through Mth transition signals at the point of time of a detected level transition;

(c) accumulating the number of generations of each of the first through Mth transition signals;

(d) detecting the transition signal whose generation frequency meets a predefined threshold; and

(e) selecting from the N data bits, K data bits corresponding to the detected transition signal.

17. The program storage device of claim 16, wherein M is 3.

18. The program storage device of claim 16, further comprising instructions for performing the step of initializing the accumulating process upon detecting a transition signal.

19. The program storage device of claim 17, wherein the instructions for performing step (e) comprise instructions for performing the steps of:

selecting K oversampled data bits by one bit of a three-times oversampling position (3P+2) corresponding to the first transition signal when the first transition signal is detected in step (d);

selecting K oversampled data bits by one bit of an three times oversampling position (3P) corresponding to the second transition signal when the second transition signal is detected in step (d); and

selecting K oversampled data bits by one bit of a three times oversampling position (3P+1) corresponding to the third transition signal when third transition signal is detected in step (d).

20. The program storage device of claim 16, wherein the instructions for performing step (e) comprise instructions for performing the steps of generating a state signal comprising a predetermined value based on the detected transition signal in step (d) and selecting the N data bits based on the value of the state signal.

21. A circuit for recovering data, the circuit comprising:

a first circuit for performing an M times oversampling on a block of input serial data using N phase clock signals having different delay times and outputting N data bits in parallel;

a second circuit for detecting a transition in a level between adjacent ones of the N data bits and outputting one of a first through Mth transition signals at the point of time of a detected level transition;

a third circuit for accumulating the number of generations of each of the first through Mth transition signals;

a fourth circuit for detecting the transition signal whose generation frequency meets a predefined threshold; and

a fifth circuit for selecting from the N data bits, K data bits corresponding to the detected transition signal.